In Application Serial No. 10/659,547
Filed September 9,2003

DECLARATION OF DAVID R. EVANS UNDER 37 CFR §1.132

I, David Russell Evans, Ph.D., hereby declare as follows:

1. My residence address is 7574 S.W. 179th Place, Beaverton, Oregon 97007.

2. Since April 1, 1999 I have been employed by Sharp Laboratories of America, Inc. ("SLA"), 5700 N.W. Pacific Rim Boulevard, Camas, Washington 98607, and between 1993 and April 1, 1999 I was employed by SLA's predecessor company, Sharp Microelectronics Technology, Inc. ("SMT"), located at the same address. My titles at SMT (until April 1, 1999) were, originally, Principal Engineer and, later, Senior Member of the Technical Staff, and my title at SLA, since April 1, 1999, is Senior Manager. My responsibilities include developing advanced process technologies to improve microelectronics fabrication. My technical experience is detailed in the attached CV.

3. I have read the claims for the patent application in question, Hsu et al., Serial Number 10/659,547 (the Applicant), entitled "Conductive Metal Oxide Gate Ferroelectric Memory Transistor". I have read the relevant parts of the Office Action dated July 22, 2005, where claims 1, 3-5, and 11-12 have been rejected as anticipated by Gnadinger (6,674,110), where claims 2 and 6 have been rejected as obvious by the combination of Gnadinger and Willer (6,538,273), where claims 7-10 have been rejected as obvious by the combination of Gnadinger and Moon (5,744,374), where claims 13 and 15-20 have been rejected as obvious by the combination of Gnadinger and Sakai (2003/0067022), and where claim 14 has been rejected as obvious by the combination of Gnadinger, Willer, and Sakai. I have read the relevant sections from all prior art references.

4. The Office Action, on pages 2 and 3, claims that Gnadinger discloses a device made from conductive oxide layers. I can unequivocally state that none of the materials used in Gnadinger's interfacial layer 31 have conductive properties. Each one

of these materials includes Si and oxygen components. Materials made from Si and oxygen may be generally referred to as silicates, which although they may be crystalline in the present context are generally glasses or glass-like material. Crystalline slilicates and/or silicate glasses, even if they contain metal or rare earth elements, are widely known to be electrically non-conductive. One other point, Gnadinger's structure is the same, in principle, as a conventional thin-film transistor (TFT) structure that uses an insulator (gate oxide) between the gate electrode and the channel in the active Si region. The purpose of the silicate material in this Gnadinger's structure both conceptually and practically is completely different than that envisioned in Hsu's invention. As such, the usage Gnadinger teaches in his patent does not anticipate the concept taught by Hsu and should not be considered as prior art.

Claims 1 and 5 appears to be distinguishable from Gnadinger because these claims list materials that are not mentioned anywhere in the Gnadinger patent. Claim 21 can be distinguished from Gnadinger because none of the materials listed by Gnadinger have a lattice structure that is similar (that can be matched) to the lattice structure of any ferroelectric material with which I am familiar. Claim 24 can be distinguished from Gnadinger since the claim describes a conductive oxide layer made without Si. All of Gnadinger's interfacial materials include Si. Claims 26 and 27 can be distinguished from Gnadinger on the simple fact, as I stated above, that Gnadinger does not disclose conductive oxide materials.

5. Willer discloses a completely different ferroelectric transistor structure from either the Applicant or Gnadinger, one that replaces the conventional (insulating) gate dielectric material with a Schottky diode. It would make no sense to combine the Gnadinger and Willer references because they address the same problem with contradictory solutions and materials. The difference in materials and structures are a result of different principles of operation. It is unlikely that an expert would seek to combine references that work in accordance with different principles. One other thing is clear to me. If the Gnadinger and Willer devices are combined, they do not disclose the Applicant's conductive oxide materials, and they do not suggest a principle of operation that would rely upon a conductive oxide gate separator.

6. Moon describes a Y_2O_3 material that is used as a gate insulator. Like the silicates disclosed by Gnadinger, Moon's gate insulator is not an electrically conductive material. Therefore, even if these references are combined, they do not describe the Applicant's ferroelectric transistor that uses a conductive oxide material between the ferroelectric layer and the channel region.

7. Sakai appears to be primarily concerned with fabrication process. I am struck by the difference in geometries between the Gnadinger and Sakai structures. It is not apparent to me that an expert would find any use in integrating Sakai's process details into the fabrication of Gnadinger's structure. However, even if these two disclosures are combined, the combination does not suggest to an expert that a ferroelectric transistor can be made using a conductive oxide in place of a conventional gate oxide or gate insulator.

8. In summary, none of the references, including the Gnadinger reference upon which the PTO Examiner places so much reliance, describes the use of a conductive oxide material that can be used in place of a gate insulator, between a ferroelectric layer and a channel region in the substrate. I have mentioned above, that there appears to be little reason the combine the references that are cited in the Office Action. However, even if the references are combined together, that combination would not lead an expert such as myself to imagine the use the Applicant's conductive oxide.

9. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful, false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful, false statements may jeopardize the validity of the application or any patent issuing thereon.

31/March/2006
Date

David R. Evans

David Russell Evans

Professional Education:

1981 Ph. D. in Physical Chemistry, Iowa State University, Ames, Iowa. Dissertation: "A Comparative Study of Classical and Quantal Approaches to Thermal and Diffusive Transport in a Dilute Atom-Diatom Binary Mixture"

1974 B. S. in Chemistry, Summa Cum Laude, (GPA 3.98) University of Missouri-Rolla, Rolla, Missouri.

Employment History:

5/1999 - Present

Sr. Manager, Dept. 5, SHARP Laboratories of America, Inc.

Responsible for project management and technical guidance of advanced resistive memory project. Previously, directed CVD copper interconnect research and development. In addition, manage chemical synthesis and associated material development. Directly responsible for advanced CMP research directed toward novel device structures, advanced perovskite materials, noble metals, nanostructures, and sensors.

5/1994 – 5/1999

Sr. Member of Technical Staff, Process Technology Laboratory, SHARP Microelectronics Technology, Inc.

Major responsibility was research and development of chemical mechanical polishing (CMP) of copper for advanced interconnect and dielectric materials for shallow trench isolation and related device structures.

11/1988 - 5/1994

Principal Engineer, Integrated Circuit Operations, Tektronix, Inc.

Major responsibility was thin film development and manufacturing, primarily for use as diffusion barriers and thin film resistors.

11/1986 - 11/1988

Principal Engineer, Liquid Crystal Strategic Program Unit, Tektronix, Inc.

Major responsibility was large area photolithography for optical shutters and passive matrix flat panel displays.

10/1980 - 11/1986

Sr. Development Engineer, Bipolar Process Development Dept., Tektronix, Inc.

Major responsibility was plasma etching and deposition. Implemented the first plasma etch processes for integrated circuit fabrication in Tektronix.

Teaching Experience:

9/1994 – 10/2004

Adjunct Faculty-Oregon Graduate Institute of Oregon Health and Science University

Graduate level course, Microelectronics Fabrication I, ECE 560, during fall term: The course covers semiconductor materials, crystal structure and growth, thermal oxidation, ion implantation and diffusion. It is part of a one-year sequence in semiconductor processing that typically is taken both by matriculating graduate students from and working professionals drawn from local industry.

3/1981 – 5/1981

Instructor-Iowa State University

Undergraduate level course, Physical Chemistry: The course covered chemical reaction kinetics, kinetic theory of gases, transport theory, x-ray diffraction and crystal structure. Prepared all lectures and exams.

Refereed Journal and Proceedings Publications:

David R. Evans and Michael R. Oliver, Chemical Mechanical Planarization-Integration, Technology and Reliability, Mater. Res. Soc., PV-867, Warrendale, PA, pg. 189, 2005 (invited). "Abrasive Contribution to CMP Friction"

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T. K. Li, S. T. Hsu, Bruce D. Ulrich, and David R. Evans, *IEEE Trans. on Elec. Dev.*, 50(11), 2280, 2003. "The Thermal Stability of One-Transistor Ferroelectric Memory with Pt-$Pb_5Ge_3O_{11}$-Ir-Poly-SiO_2-Si Gate Stack"

T. K. Li, S. T. Hsu, B. Ulrich, L. Stecker, D. Evans, and J. J. Lee, *IEEE Elec. Dev. Lett.*, 23(6), 339, 2002. "One-transistor Ferroelectric Memory with Pt/$Pb_5Ge_3O_{11}$/Ir/Poly-Si/SiO_2/Si Gate Stack"

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W. Zhuang, L. Charneski, D. Evans, S. T. Hsu, Z. Tang and A. Guloy, *J. de Physique IV, EUROCVD 13*, Aug. 2001. "CVD Copper Thin Film Deposition Using (α-methylstyrene)Cu(I)(hfac)"

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David R. Evans, Michael R. Oliver, and Mike Kulus, Chemical Mechanical Planarizarion IV, Electrochem. Soc. PV-2000-26, Pennington, NJ, pg. 122, 2001. "Morphology Evolution during Copper CMP: Comparison of Fixed Abrasive and Conventional Pads"

Weiwei Zhuang, Lawrence J. Charneski, David R. Evans, and Sheng Teng Hsu, Advanced Metallization Conference 1999, Mater. Res. Soc., Warrendale, PA, pg. 213, 2000. "New Copper Precursor for Chemical Vapor Deposition of Pure Copper Thin Films"

Y. Ma, D. R. Evans, T. Nguyen, Y. Ono, and S. T. Hsu, *IEEE Elec. Dev. Lett.*, 20(5), 254, 1999. "Fabrication and Characterization of Sub-Quarter-Micron MOSFET's with a Copper Gate Electrode"

Yanjun Ma, Douglas J. Tweet, Larry Charneski, and David R. Evans, Advanced Metallization Conference in 1998, Mater. Res. Soc., Warrendale, PA, pg. 357, 1999. "Density Oscillation in Sputtered Tantalum Nitride Barrier Metal Thin Films"

T. Nguyen, L. J. Charneski, and D. R. Evans, *J. of the Electrochem. Soc.*, 144(10), 3634, 1997. "Temperature Dependence of the Morphology of Copper Sputter Deposited on TiN Coated Substrates"

D. R. Evans, Chemical Mechanical Planarizarion I, Electrochem. Soc. PV-96-22, Pennington, NJ, pg. 70, 1997. "Electrochemical Interaction between Copper and Barrier Materials During Chemical Mechanical Polishing"

D. R. Evans, Y. Ono, J.-F. Wang, A. R. Sethuraman, amd L. M. Cook, Advanced Metallization and Interconnect Systems for ULSI Applications in 1995, Mater. Res. Soc., Warrendale, PA, pg. 717, 1996. "Yield and Defect Characterization of CMP Copper Metallization"

Y. Ono, D. R. Evans, and T. Nguyen, Advanced Metallization and Interconnect Systems for ULSI Applications in 1995, Mater. Res. Soc., Warrendale, PA, pg. 165, 1996. "Comparison of Electromigration Characteristics of Pure Copper and Aluminum Alloy Metallizations"

Z. Karim and D. Evans, Advanced Metallization and Interconnect Systems for ULSI Applications in 1995, Mater. Res. Soc., Warrendale, PA, pg. 101, 1996. "Improvement of the Dielectric Properties of Silsesquioxane Based Spin-on-Polymer by Plasma Treatment and Other Novel Techniques"

David M. Leet and David R. Evans, *J. of the Electrochem. Soc.*, 142(6), 2013, 1995. "3% Ti-Tungsten Barriers II: The Effect of Deposition Temperature and Nitrogen Inclusion"

J. Wu, J. D. Parsons, and D. R. Evans, *J. of the Electrochem. Soc.*, 142(2), 669, 1995. "Sulfur Hexafluoride Reactive Ion Etching of (111) β-SiC Epitaxial Layers Grown on (111) TiC Substrates"

J. Wu, J. D. Parsons, and D. R. Evans, *J. of the Electrochem. Soc.*, 141(10), 2915, 1994. "Reactive Ion Etching of (111) β-SiC Epitaxial Layers on (111) TiC Substrates in CF_4+O_2+Ar"

David M. Leet and David R. Evans, *J. of the Electrochem. Soc.*, 141(7), 1867, 1994. "3% Ti-Tungsten Barriers I: A Discussion of the Role of the A15 Structure"

D. R. Evans, SOTAPOCS XIII and Metallization of III-V Compound Semiconductors, Electrochem. Soc. PV-91-1, Pennington, NJ, pg. 354, 1991. "Sputter-Deposited Nitrogen-doped Titanium-Tungsten: Material and Etching Characteristics"

J. Dwire, D. Evans, D. Fuoss, and D. Hoy, SOTAPOCS XIII and Metallization of III-V Compound Semiconductors, Electrochem. Soc. PV-91-1, Pennington, NJ, pg. 346, 1991. "Defect Characterization for a Two-layer Gold I. C. Interconnect"

D. R. Evans, G. T. Evans, and D. K. Hoffman, *J. of Chem. Phys.*, 93(12), 8816, 1990. "Chattering Collisions and Their Effects on Gas Phase Rotational Energy Relaxation Cross Sections"

D. J. Economou, D. R. Evans, and R. C. Alkire, *J. of the Electrochem. Soc.*, 135(3), 756, 1988. "A Time Average Model of the RF Plasma Sheath"

R. G. Cole, D. R. Evans, and D. K. Hoffman, *J. of Chem. Phys.*, 82(4), 2061, 1985. "A Renormalized Theory of Dilute Molecular Gases: Chattering"

G. T. Evans and D. R. Evans, *J. of Chem. Phys.*, 81(12), 6039, 1984. "Kinetic Theory of Rotational Relaxation in Liquids: Smooth Spherocylinders and Rough Sphere Models"

D. R. Evans, Plasma Processing IV, Electrochem. Soc. PV-83-10, Pennington, NJ, pg. 199, 1983. "Dry Etched Vias for Two Layer Interconnect on High Density Bipolar Integrated Circuits"

D. E. Fitz, D. J. Kouri, W.-K. Liu, F. R. McCourt, D. Evans, and D. K. Hoffman, *J. of Phys. Chem.*, 86(7), 1087, 1982. "The Utility of the CS and IOS Approximations for Calculating Generalized Phenomenological Cross Sections in Atom-Diatom Systems"

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Conference Presentations:

John F. Conley, Jr., D. Evans, W. Gao, L. Stecker, and Y. Ono, in collaboration with D. McClain, C. Fei, and J. Jiao, *MRS Meeting-Spring 2005*, San Francisco, CA, Mar. 28-31, 2005. "Self Catalyzed Growth of Nanocones During DC Magnetron Sputtering of an ITO Targets"

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Michael R. Oliver and David R. Evans, *MRS Meeting-Spring 2005*, San Francisco, CA, Mar. 28-31, 2005. "Abrasive Contribution to CMP Friction"

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David R. Evans, *MRS Meeting-Spring 2004*, San Francisco, CA, Apr. 12-16, 2004. "Cerium Oxide – Observations and Analysis" (*invited*)

T. K. Li, S. T. Hsu, B. Ulrich, and D. Evans, *MRS Meeting-Fall 2003*, Boston, MA, Dec. 1-5, 2003. "Characteristics and Calculation of One-Transistor Memory Devices"

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W. Meyer, D. R. Evans, and R. Solanki, *MRS Meeting-Spring 2003*, San Francisco, CA, Apr. 21-25, 2003. "Blech Length versus Titanium-Nitride Barrier Thickness"

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W. W. Zhuang, W. Pan, Sheng Teng Hsu, D. R. Evans, F. Zhang, S. Liu, N. Wu, and A. Ignatiev, *Symp. on Integrated Ferroelectrics*, Colorado Springs, CO, Mar. 9-12, 2003. "Introduction to the Resistance Switch Properties of PCMO Spin-Coating Thin Films"

David Evans, *2003 CMP for ULSI Multilevel Interconnection Conf. (CMP-MIC)*, Marina Del Ray, CA, Feb. 21, 2003 (invited). "Emergent CMP Applications"

T. K. Li, S. T. Hsu, B. Ulrich, F. Zhang, D. and D. Evans, *MRS Meeting-Fall 2002*, Boston, MA, Dec. 1-5, 2002. "Integration Processes and Properties of One-transistor Memory Devices"

W. Zhuang, J. Conley, Y. Ono, D. Evans, and R. Solanki, *Int. Joint Conf. on the Applications of Ferroelectrics*, Nara, Japan, May 28-Jun. 1, 2002. "Hafnium Nitrate Precursor Synthesis and Hafnium Oxide Thin Film Properties"

T. K. Li, S. T. Hsu, B. Ulrich, and D. Evans, *Int. Joint Conf. on the Applications of Ferroelectrics*, Nara, Japan, May 28-Jun. 1, 2002. "Comparison of MFOS and MFMOS One-transistor Memory Devices"

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David R. Evans, *2000 Clarkson Univ. Int. CMP Symp.*, Lake Placid, NY, Aug. 13-17, 2000. "CMP for Advanced Front End Processing"

Fengyan Zhang, Sheng Teng Hsu, Hong Ying, David Evans, Shigeo Ohnishi, and Wendong Zhen, *IEEE Int. Symp. on the Applications of Ferroelectrics*, Honolulu, HA, July 31-Aug. 2, 2000. "Integration of SBT Thin Film into MFMOS Structure for One Transistor Memory Applications"

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Hongning Yang, Douglas Tweet, Lisa Stecker, Wei Pan, David R. Evans, and Sheng Teng Hsu, *ECS Meeting-Spring 2000*, Toronto, ON, Canada, May 14-19, 2000. "Development of PECVD Low-κ Carbon-doped Silicon Oxide Using SiH_4 Based Precursor"

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David R. Evans, *AVS 1st Int. Conf. on Microelectronics and Interfaces*, Santa Clara, CA, Feb. 9, 2000 (invited). "Electrochemical and Associated Interactions in an Integrated Polished Copper Interconnect Process"

Yanjun Ma, Yoshi Ono, Lisa Stecker, David R. Evans, and S. T. Hsu, *IEEE Int. Elec. Dev. Mtg. 1999*, Washington, DC, Dec. 5-8, 1999. "Zirconium Oxide Based Gate Dielectrics with Equivalent Oxide Thickness of Less Than 1.0 nm and Performance of Submicron MOSFET using a Nitride Gate Replacement Process"

David Evans, Bruce Ulrich, Michael Oliver, and Sharath Hosali, *1999 Clarkson Univ. Int. CMP Symp.*, Lake Placid, NY, Aug. 8-11, 1999. "Polysilicon Polish Stop for STI CMP Using Experimental Slurry"

David J. Stein, Dale L. Hetherington, James E. Stevens, Michael R. Oliver, Sharath D. Hosali, and David R. Evans, *1999 Clarkson Univ. Int. CMP Symp.*, Lake Placid, NY, Aug. 8-11, 1999. "Oxide CMP Using Ceria-based Slurries"

S. T. Hsu, D. Evans, T. Nguyen, and H. Yang, *Sixth Symp. on Nano Device Technology*, National Nano Device Laboratories, National Science Council, Taiwan, ROC, May 12-13, 1999. "Cu/a-F:C Interconnect Technology"

D. R. Evans, *1999 Int. Conf. On GaAs Manufacturing Technology*, Vancouver, BC, Canada, Apr. 19, 1999 (invited). "The Role of CMP in the Fabrication of Advanced Interconnect"

H. Yang, D. R. Evans, T. Nguyen, L. Stecker, B. Ulrich, and S. T. Hsu, *MRS Meeting-Spring 1999*, San Francisco, CA, Apr. 5-9, 1999. "Multilevel Damascene Interconnection in Integration of MOCVD Cu and Low-κ Fluorinated Amorphous Carbon"

David J. Stein, Dale L. Hetherington, James E. Stevens, Michael R. Oliver, Sharath D. Hosali, and David R. Evans, *MRS Meeting-Spring 1999*, San Francisco, CA, Apr. 5-9, 1999. "Investigation of a Self-stopping ILD CMP System"

H. Yang, D. R. Evans, T. Nguyen, L. Stecker, B. Ulrich, and S. T. Hsu, *MRS Meeting-Spring 1999*, San Francisco, CA, Apr. 5-9, 1999. "Multilevel Damascene Interconnection in Integration of MOCVD Cu and Low-κ Fluorinated Amorphous Carbon"

Tue Nguyen, Hongning Yang, David Evans, Bruce Ulrich, Lisa Stecker, and Sheng Teng Hsu, *1998 Advanced Metallization Conf.*, Colorado Springs, CO, Oct. 6-8, 1998. "Integration of MOCVD Copper and Low-κ Fluorinated Amorphous Carbon in Single and Dual Damascene Interconnection"

David Evans, *CMP Technology for ULSI Interconnection Seminar at SEMICON West*, San Francisco, CA, Jul. 14, 1998 (invited). "Pattern Dependence and Planarization for Shallow Trench Isolation"

T. Nguyen, H. Yang, D. R. Evans, and S. T. Hsu, *1998 VLSI Multilevel Interconnection Conf. (VMIC)*, Santa Clara, CA, Jun. 16-18, 1998, pg. 31. "Integration of MOCVD Copper and Low-κ Fluorinated Amorphous Carbon in Single Damascene Structures"

H. Yang, D. Evans, J. Takason and T. Hara, *ECS Meeting-Spring 1998*, San Diego, CA, May 5, 1998 "Thermal Stability of Organic Interlayers with Low Dielectric Constant"

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Tue Nguyen, Dave Evans, and Sheng Teng Hsu, *1997 VLSI Multilevel Interconnection Conf. (VMIC)*, Santa Clara, CA, Jun. 10-12, 1997. "Integration of MOCVD Copper Metallization with SIMOX Devices"

D. R. Evans, *2nd Int. CMP Symp.*, Tokyo, Japan, Dec. 2, 1996 (invited). "Electrochemical Interaction between Barrier Metals and Copper During Chemical Mechanical Polishing"

T. Nguyen, B. D. Ulrich, L. R. Allen, and D. R. Evans, *IEEE Symp. on VLSI Technology*, pg. 118, Honolulu, HA, Jun. 11-13, 1996. "A Novel Damascene Process for One Mask Via/Interconnect Formation"

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Z. Karim and D. Evans, *1996 Dielectrics for ULSI Multilevel Interconnection Conf. (DUMIC)*, Santa Clara, CA, Feb. 20, 1996. "Integration Issues for Use of Silsesquioxane Based Spin-on-Polymer with Sub-half Micron Technology"

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T. Nguyen and D. Evans, *MRS Meeting-Fall 1994*, Boston, MA, Nov. 27-Dec. 2, 1994. "Stress and Adhesion of CVD Copper and TiN"

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Other Publications:

D. R. Evans in *Tutorial Session Notes: "Recent Advances in Chemical Mechanical Planarization Technology", MRS Meeting-Spring 2005, San Francisco, CA, Mar. 28-31, 2005.* "CMP Integration"

D. R. Evans in Chemical-Mechanical Planarization of Semiconductor Materials (Springer Series in Materials Science, 69), ed. M. R. Oliver, *Springer-Verlag*, Berlin/Heidelberg, Mar. 2004. "Metal Polishing"

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Continuing Education and Other Skills:

Broad experience related to collaborative research and development efforts with universities, government laboratories, and private companies. This includes writing legally binding contracts and statements of work, administering grants, and managing collaborative efforts of a more informal nature.

Taken several electrical engineering courses through Oregon State University, Portland State University, and University of Portland that cover fundamental circuits and devices. Additionally, have participated in several work-related technical and management training programs.

Proficient in applied mathematics and algorithm construction.